REMARKS

Upon entry of the attached amendments, claims 16-30 are pending in the application. Claims 1-12 have been canceled without prejudice, waiver, or disclaimer. Original claims 13-15 were canceled in a previous amendment. Claims 16-30 have been added. The subject matter of claims 16-30 is supported in the apparatus, method, and timing diagram of FIGs. 2, 3, and 4, respectively and the related detailed description. Consequently, Applicant submits no new matter is added.

The rejections of canceled claims 1-12 are rendered moot in light of the cancellation of those claims. The following remarks will distinguish Applicant's claimed apparatus and method from the cited art of record.

I. Claims 16-19

Applicant's canceled claims 1-3 were rejected as being anticipated by U.S. Patent 6,230,257 to Roussel *et al.* Applicant respectfully submits that new claims 16-19 are not anticipated by U.S. Patent 6,230,257 to Roussel *et al.*, hereafter the '257 patent, for at least the reason that the '257 patent fails to disclose, teach, or suggest each element in the claims.

For convenience of analysis, new independent claim 16 is repeated below in its entirety.

> 1. An apparatus, comprising:
> a multiply accumulate (MAC) unit coupled to operand busses at respective operand inputs, the MAC unit configured to latch a first multiple-bit data value during a first cycle and initiate execution of the MAC functions on the first multiple-bit data value during the next subsequent cycle while latching a second multiple-bit data value, the MAC unit further configured to supply a first MAC result responsive to the first multiple-bit data value on a result bus once the first MAC result is available and latch a second MAC result responsive to the second multiple-bit data value;
> a register coupled to the result bus configured to latch the first MAC result; and
> ***a miscellaneous-logic unit coupled between the result bus and the register***, the miscellaneous-logic unit ***configured to generate first and second control signals responsive to certain exceptional conditions***, wherein when the first control signal is asserted the MAC unit

> supplies the second MAC result on the result bus, when the second control signal is asserted the first MAC result is driven from the register onto the result bus, and wherein when the second control signal is not asserted a miscellaneous-unit generated result is driven onto the result bus.

(Applicant's independent claim 16 - *emphasis added.*)

Applicant respectfully asserts that the '257 patent does not disclose, teach, or suggest at least the emphasized elements/limitations of claim 16 as shown above. Consequently, claim 16 is allowable. Accordingly, for at least this reason, Applicant respectfully submits that Applicant's claim 16 and claims 17-19 that depend therefrom are allowable over the '257 patent.

Applicant's canceled claims 4-15 were rejected as being allegedly unpatentable over the '257 patent in view of U.S. Patent 6,038,652 to Phillips et al., hereafter the '652 patent. Applicant respectfully submits that new claims 16-19 are not rendered obvious over the combination of the '257 and '652 patents for at least the reason that the combination does not disclose, teach, or suggest at least the emphasized elements/limitations of claim 16 as shown above. Accordingly, for at least this reason, Applicant respectfully submits that claims 16-19 are allowable over the cited art of record.

II. Claims 20-25

For convenience of analysis, new independent claim 20 is repeated below in its entirety.

> 20. A method for performing single-instruction multiple-data instructions comprising:
> applying a plurality of data values on an operand bus for two consecutive cycles;
> latching a first data value in a multiply-accumulate (MAC) unit during a first cycle;
> initiating execution of the multiply and accumulate functions on the first data value and latching a second data value in the MAC unit during a second cycle;
> deferring a first MAC unit result responsive to the first data value;

initiating execution of the multiply and accumulate functions on the second data value during a cycle subsequent to the second cycle to generate a second MAC unit result; and

generating a plurality of control signals responsive to the first data value, the second data value, and exceptional conditions identified by the MAC unit.

(Applicant's independent claim 20 - *emphasis added.*)

Applicant's canceled claims 4-15 were rejected as being allegedly unpatentable over the '257 patent in view of the '652 patent. Applicant respectfully submits that new claims 20-25 are not rendered obvious over the combination of the '257 and '652 patents for at least the reason that the combination does not disclose, teach, or suggest at least the emphasized elements/limitations of claim 20 as shown above. Accordingly, for at least this reason, Applicant respectfully submits that claims 20-25 are allowable over the cited art of record.

III. Claims 26-30

For convenience of analysis, new independent claim 26 is repeated below in its entirety.

26. An apparatus comprising:

means for producing a plurality of control signals responsive to a first data value, a second data value, and exceptional conditions, wherein the exceptional conditions result from the execution of a multiply-accumulate (MAC) unit over the first and second data values; and

means for arranging a combination selected from a first MAC unit result, a second MAC unit result, and a representation of an exceptional condition responsive to the plurality of control signals.

(Applicant's independent claim 26 - *emphasis added.*)

Applicant's canceled claims 4-15 were rejected as being allegedly unpatentable over the '257 patent in view of the '652 patent. Applicant respectfully submits that new claims 26-30 are not rendered obvious over the combination of the '257 and '652 patents for at least the reason that the combination does not disclose, teach, or suggest at

least the emphasized elements/limitations of claim 26 as shown above. Accordingly, for at least this reason, Applicant respectfully submits that claims 26-30 are allowable over the cited art of record.

CONCLUSION

In summary, Applicant respectfully submits that presently pending claims 16-30 are allowable and the present application is in condition for allowance. Accordingly, a Notice of Allowance is respectfully solicited. Should the Examiner have any comments regarding the Applicant's response or intends to dispose of this matter in a manner other than a Notice of Allowance, Applicant requests that the Examiner telephone Applicant's undersigned attorney.

Respectfully submitted,

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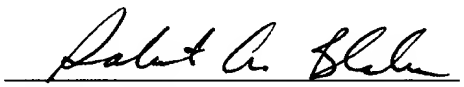
By: 

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